a synchronous circuit;

an asynchronous circuit;

A1 Cont.

an input register circuit connected to said synchronous circuit and said asynchronous circuit, said input register circuit having a terminal receiving a first control clock signal for controlling data transfer;

an output register circuit connected to said synchronous circuit and said asynchronous circuit, said output register circuit having a terminal receiving a second control clock signal for controlling data transfer; and

a sequence controller;

said input register circuit storing data of said synchronous circuit for processing in said asynchronous circuit;

said output register circuit storing data of said asynchronous circuit for further processing in said synchronous circuit; and

said sequence controller connected to said asynchronous circuit for generating the first control clock signal and the

A1

second control clock signal in dependence on a duration required for the data to be processed in said asynchronous circuit.

Claim 6(amended). A method for operating an integrated circuit, the method which comprises:

A2

activating a first control clock signal to transfer data from a synchronous circuit into an input register circuit;

transferring the data from the input register circuit into an asynchronous circuit and processing the data in the asynchronous circuit to obtain processed data;

with a sequence controller, inactivating the first control clock signal within the duration required for the data to be processed in the asynchronous circuit; and

not earlier than a completion of the duration required for the data to be processed in the asynchronous circuit, using a second control clock signal to trigger transfer of the processed data into an output register circuit.

Claim 7(amended). The method according to claim 6, which comprises:

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providing a terminal for receiving a clock signal having an active state and an inactive state;

A2 Cont.

providing a controllable switch for switchably connecting together the terminal for receiving the clock signal and a terminal receiving the first control clock signal;

inactivating the first control clock signal by opening the controllable switch; and

using the sequence controller to close the controllable switch in the inactive state of the clock signal.